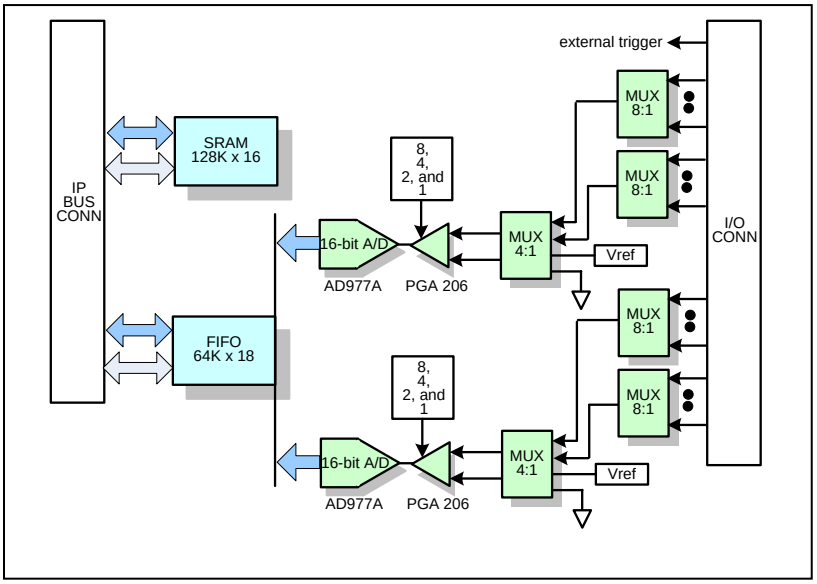
IP-AD-3216

IP Module

IP 16 bit A/D converter, 2 A/D modules, 32 multiplexed input channels

Features

- 16-bit AD977 A/D converter module
- 2 A/D modules each with 16 single-ended or 8 differential multiplexed A/D inputs for a total of or 32 single-ended or 16 differential analog inputs
- Acquisition time of 100Ksps
- Programmable ranges: ±10VDC, 0-10VDC, ±5VDC, 0-5VDC, ±3.3VDC, and 0-4VDC
- 64Kx18 FIFO enables burst mode or continuous sampling at lower throughput
- Channel 128K x 16 SRAM enables storage of gain, calibration and input mode selection per input channel.
- Differential inputs can be configured for single-ended, differential modes, or calibration modes (Vref or GND)
- Pre-trigger and post trigger acquisition
- Sampling clock selected from one of the following sources:
  - Internal divider (IPCLK/N), or
  - IPSTROBE,
- Trigger event selected from one of the following sources:
  - Write to IP register,
  - IPSTROBE, or
  - External trigger
- 8 or 32 MHz clock
- 2 interrupts and 2 slave DMA IP bus lines
- VITA 4 compliant
- 32 bytes of EEPROM are used for board ID



Block Diagram and Operational Overview

The **IP-AD-3216** has four CMOS analog multiplexers that are fault protected. Each multiplexer has 8 inputs and one common output. These outputs are acquired by a four input differential multiplexer.

The differential multiplexer inputs can then be configured for single-ended, differential modes, or calibration modes. These outputs then go to a PGA where the gain can be set for 1, 2, 4, and 8.

When the acquisition is started the two A/D converters acquire the data simultaneously from the multiplexers. The data is stored in a 16-bit FIFO in an interleave matter reading group #1 (odd channel) first then group #2 (even channel). Further acquisitions before the trigger will result in the earliest data being discarded, thus maintaining the most recent data in the FIFO.

Once the trigger event is seen, no more data is discarded from the FIFO, and the acquisition proceeds until the FIFO is full. At this point, the acquisition stops, and the HOST can read the data from the IP. Interrupts can be sent to the HOST at Event and at acquisition finished.

If desired, such as for a continuous acquisition, data can be read from the FIFO while acquisition is in progress, supporting continuous streaming

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Applications:

This is a perfect solution for:

- Process control,
- Industrial control, or
- Precision instrumentation

Software Support:

The **IP-ADM-2100-32CH** is supported under *Windows NT* / 2000 by two sample programs, which are supplied with the IP in the board support package. Both examples are designed to work with an IP-type carrier from ALPHI, such as the PCI-4IPM.

One sample program, called SnapShot, fully exercises the IP module in pre- and post-trigger modes, and displays the data to the screen. Data can be stored to a file and can be reloaded in the program at a later time.

The second program, called DrawIpAdc, operates the IP in continuous mode, and displays the data to the screen.

Full source to both HOST DSP code and the applications are provided.

AD977A A/D Specifications:

- 16-bit, successive approximation A/D
- Fast throughput rate of 100Ksps
- Single power supply +5VDC
- Internal or external voltage references
- On-chip clock
- Analog input voltage ranges: ±10VDC, 0-10VDC, ±5VDC, 0-5VDC, ±3.3VDC, and 0-4VDC
- Integral linearity error ±3LSB
- Differential linearity error -2LSB min to +3LSB max
- Full-scale error ±0.5%
- SNR 83dB
- Full power bandwidth 700KHz
- Over voltage recovery 150nsec

PGA206 Programmable Gain Amplifier Specifications:

- Programmable gains of 1, 2, 4, 8
- Fast settling time 3.5 µsec to 0.01%
- FET input I_B = 100pA max; eliminated I_B errors due to analog multiplexer series resistance
- Input protection ±40VDC

Industry Pack Specifications:

- Meets ANSI/VITA 4-1995
- 8/32 MHz synchronous operation
- Supports ID, 128 byte I/O, interrupt. & 8 Mbyte memory spaces
- 2 Interrupts per module
- Two passive DMA channels are possible.
- Hardware self timed per IP module
- Triggered via system reset and software control
- Jumper or software time-out function
- 5, +/-12 volt reset-able fuse per IP

Mechanical: Environmental:

- Size – VITA 4 compliant
  1.8" x 3.9" or 46 mm x 99 mm
- Power – 1.0 watt
- Vibration – 0.5G, 20-2000 Hz rand
- Shock – 20G, 11 msec, ½ sine
- Weight – 2 ounces
- MTBF – >250,000 hours

Operating Environment:

- Operating temperature
  Commercial: 0 to +70 ºC
  Optional: -25 ºC to +80 ºC
- Non-operating: -40 ºC to +85 ºC
- Airflow requirement – 5 CFM
- Humidity – 5 to 90% (non-cond)
- Altitude – 0 to 10,000 feet

VITA
Open Standards, Open Markets

Ordering Information:

Part number: IP-AD-3216 32 channel 16 bit multiplexed A/D Industry Pack Module

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