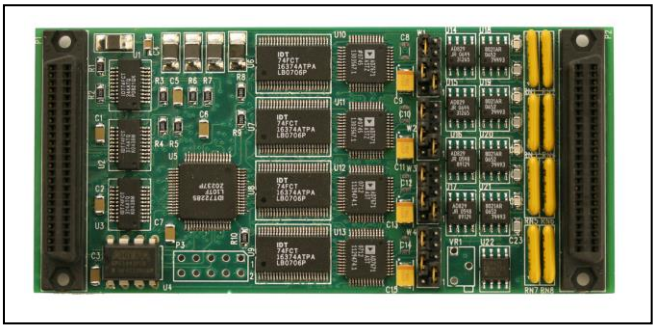
IP-AD-41M

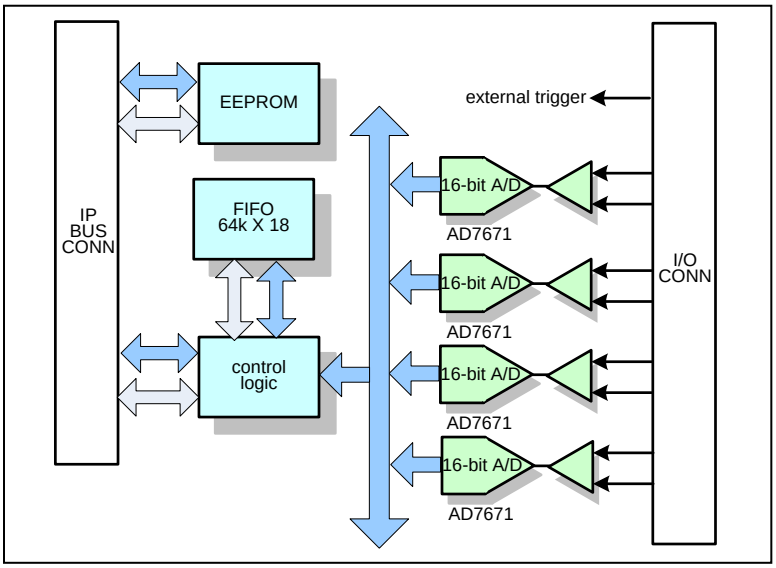
IP Module

IP 16 bit A/D converter, 4 A/D modules

Features



- 16-bit AD7671 A/D converter module
- 4 A/D modules with 4 differential A/D inputs
- Acquisition time of 1000Ksps
- Programmable ranges: ±10VDC, 0-10VDC, ±5VDC, 0-5VDC, ±2.5VDC, and 0-2.5VDC through A/D converter
- 64Kx18 FIFO enables burst mode or continuous sampling at lower throughput using control logic
- Pre-trigger and post trigger acquisition
- Sampling clock selected from one of the following sources:
  - Internal divider (IPCLK/N), or
  - IPSTROBE, or
  - External clock
- Trigger event selected from one of the following sources:
  - Write to IP register,
  - IPSTROBE, or
  - External trigger
- 8 or 32 MHz clock
- 2 interrupts and 2 slave DMA IP bus lines
- VITA 4 compliant
- 32 bytes of EEPROM are used for board ID



Block Diagram and Operational Overview

The **IP-AD-41-M** has four 16-bit A/D converters that run simultaneously at 250Ksps with front-end buffers that are fault protected. The A/D converters support unipolar and bipolar voltage inputs, and include ±10VDC, 0-10VDC, ±5VDC, 0-5VDC, ±2.5VDC, and 0-2.5VDC input ranges.

The A/D converters operate continuously at the selected sampling rate. Results are either stored in the FIFO or discarded when appropriate. Only selected channels are saved into the FIFO, so that depth per channel is proportional to number of channels saved.

The customer may desire to think of the IP module as similar to a Digital Storage Oscilloscope (DSO). A DSO can store and display several waveforms and can record signals prior to the trigger. The trigger point is completely configurable by reprogramming the FIFO's programmable empty flag.

A/D samples are acquired and stored into the 18 bit FIFO when acquisition has been started. Once the pre-trigger data has been acquired, triggering becomes active. Further, acquisition before the trigger that are seen will result in the earliest data being discarded at the same time new data is saved, thus maintaining the most recent data in the FIFO.

Once the trigger event is seen, no more data is discarded from the FIFO, and acquisition proceeds until the FIFO is full. At this point, the acquisition stops, and the HOST can read the data from the IP. Interrupts can be sent to the HOST at Event and at acquisition finished.

If desired, such as for a continuous acquisition, data can be read from the FIFO while acquisition is in progress, for continuous streaming. Unfortunately, it will not be possible to maintain a high sampling rate in this scenario due to the time constraints of the IP interface.

Alphi Technology Corporation,1898 Southern Avenue, Tempe, Arizona 85282
Telephone: 480.838.2428 Fax: 480.838.4477
Contact Email: engineering@alphitech.com Visit: www.alphitech.com

www.alphitech.com

IP-AD-41M

IP Module

Applications:

This is a perfect solution for:

- Process control,
- Industrial control, or
- Precision instrumentation

Software Support:

The **-AD-41000-4CH** is supported under *Windows NT* /2000 by two sample programs, which are supplied with the IP in the board support package. Both examples are designed to work with an IP-type carrier from ALPHI, such as the PCI-4IPM.

One sample program, called SnapShot, fully exercises the IP module in pre- and post-trigger modes, and displays the data to the screen. Data can be stored to a file and can be reloaded in the program at a later time.

The second program, called DrawIpAdc, operates the IP in continuous mode, and displays the data to the screen.

Full source to both HOST DSP code and the applications are provided.

AD7663 A/D Specifications:

- 16-bit, charge redistribution SAR, A/D operating from a single +5VDC supply
- Fast throughput rate of 1000Ksps
- Single power supply +5VDC
- On-chip clock
- Error correction internal circuits
- Analog input voltage ranges supported by an internal resistor scaler network: ±10VDC, 0-10VDC, ±5VDC, 0-5VDC, ±2.5VDC, and 0-2.5VDC
- Integral linearity error ±2.5LSB max with no missing codes
- THD -100dB typical @ 250kHz
- Full-scale bipolar error ±0.38% of FSR
- Full-scale unipolar error ±0.76% of FSR
- SNR 90dB at 250KHz typical

Buffer Amplifier Specifications:

Industry Pack Specifications:

- Meets ANSI/VITA 4-1995
- 8/32 MHz synchronous operation
- Supports ID, 128 byte I/O, interrupt. & 8 Mbyte memory spaces
- 2 Interrupts per module
- Two passive DMA channels are possible.
- Hardware self timed per IP module
- Triggered via system reset and software control
- Jumper or software time-out function
- 5, +/-12 volt reset-able fuse per IP

Mechanical: Environmental:

- Size – VITA 4 compliant
  1.8" x 3.9" or 46 mm x 99 mm
- Power – 1.0 watt
- Vibration – 0.5G, 20-2000 Hz rand
- Shock – 20G, 11 msec, ½ sine
- Weight – tbd
- MTBF – >250,000 hours

Operating Environment:

- Operating temperature
  Commercial: 0 to +70 ºC
  Optional: -25 ºC to +80 ºC
- Non-operating: -40 ºC to +85 ºC
- Airflow requirement – 5 CFM
- Humidity – 5 to 90% (non-cond)
- Altitude – 0 to 10,000 feet

VITA
Open Standards, Open Markets

Ordering Information:

Part number:	IP-AD-41M	4 channel, 16 bit, 1000ksps A/D Industry Pack Module

Alphi Technology Corporation,1898 Southern Avenue, Tempe, Arizona 85282
Telephone: 480.838.2428 Fax: 480.838.4477
Contact Email: engineering@alphitech.com Visit: www.alphitech.com

Alphi Technology Corporation,1898 Southern Avenue, Tempe, Arizona 85282
Telephone: 480.838.2428 Fax: 480.838.4477
Contact Email: engineering@alphitech.com Visit: www.alphitech.com